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# Thermo-Mechanical Analysis of GaAs Devices Under Temperature-Humidity-Bias Testing

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## Abstract

Accelerated life tests on microelectronic devices are needed to estimate their degradation under severe environment. THB (Temperature Humidity Bias) [1] at 85°C and 85%RH (relative humidity) is commonly used for reliability studies. Empirical acceleration laws, used for THB test take into account the temperature change (from 22°C to 85°C), but they do not quantify its impact of the corresponding thermo-elastic stress which it adds to the residual stress in the die and of possible microstructure changes. The aim of this work is to determine the thermo-mechanical stresses induced in the active layer of a Gallium Arsenide (GaAs) chip by the THB test. They are due to the mismatch in Coefficients of Thermal Expansion (CTE) between the stack of thin film materials used as metallurgic interconnection and the intermediate dielectric layers above the active area of the chip. To estimate this stress, first layers thicknesses measurement have been made with various techniques; second few configurations have been used to simulate heating and finally “complete” 2D Finite Element Analysis (FEA) has been performed. Elastic and thermo-physical materials data come from the literature. The results indicate compression of metal gate (Ti/Al/Au) and tensile stress concentration in the SiN<sub>x</sub> passivation layer. The outcomes is compared with THB test results from [2] and suggests that stress induced by heating must be considered to explain failure during THB test.

## 1. Introduction

For Space applications, devices are generally encapsulated by hermetic packaging to prevent any pollution or moisture penetration during the storage on ground of the equipment that could damage the microelectronic devices. At die level, life tests are performed to validate the use of a chip technology.

In the case of non-hermetic packaging and in addition to standard life tests, damp humidity testing at 85°C and 85% RH for several hours should be performed to access the impact of moisture on the device reliability. This test can be performed with or without DC bias applied to the devices and bias may be direct (a current flows through gate) or reverse (no current).

A usual acceleration law for THB tests was published by Hallberg and Peck [3] to estimate the Mean Time To Failure (MTTF) of the devices. This empirical model takes into account the relative humidity, the bias (applied voltage) and the temperature change by using analytic formulation and experimental results. It has been validated for some silicon technologies but is not adapted

for technologies based on GaAs even if others authors have enriched it several times.

Unfortunately this model does not quantify other parameters such as the impact of temperature change on the residual stress in the die and possible microstructure change. Because of CTE mismatch between constituent layers, heating the device during THB (or during use) superimposes thermo-elastic stresses to the residual stresses initially present. The latter are mainly due to the same kind of thermo-elastic stress built up when the device was cooled from fabrication temperature to room temperature. Indeed, the stress at any time is equal to the thermo-elastic stress corresponding to the difference between manufacturing temperature and the temperature at that time. In the present paper, only the thermo-elastic stress due to the heating in THB test is considered.

A vast literature exists on this topic for multilayer structures. While the stress and reliability issues have been widely studied in metallic thin films on substrate and in adhesively bonded assemblies, the thermo-mechanical behavior of devices under aging tests has not been fully studied and understood yet. Most studies focus on the stresses induced during fabrication due to the variation of temperature, the mismatch in the CTE and depending on materials thickness and properties.

This paper presents an evaluation of thermo-mechanical stresses induced in the active part of non-hermetically packaged Monolithic Microwave Integrated Circuit (MMIC) devices dedicated for Space applications by the temperature raise during THB 85/85 test. First, the thicknesses of the different layers of materials constituting the MMIC must be evaluated, including dielectric layers and gate metallization of the transistors. Results from X-ray Photoelectron Spectroscopy (XPS) analysis and FIB-SEM cross sections (Focused Ion Beam and Scanning Electron Spectroscopy) are presented in section 2. Second, analytical models are summarized in section 3 and the numerical model based on finite element method (FEM) are described in section 4. In section 5, the models developed are used to quantify thermo-mechanical stresses induced by heating for a specific multilayer stack (GaAs/Ti/Al/Au/SiN<sub>x</sub>/SiO<sub>y</sub>/SiN<sub>x</sub>) of the gate finger area. Results are then correlated with cracks studied in [2] on non-hermetic tested devices with reverse bias.

## 2. Layer thickness measurement

The GaAs MMIC used in this study includes two 0,18μm pseudomorphic High Electron Mobility Transistors (pHEMT) and a SiN<sub>x</sub>/SiO<sub>y</sub>/SiN<sub>x</sub> Metal-Insulator-Metal (MIM) capacitor. According to the

foundry process description,  $\text{SiN}_x$  and  $\text{SiO}_y$  are respectively 0,15 $\mu\text{m}$  and 0,8 $\mu\text{m}$  thick.

An investigation has been made to check these thicknesses by using two main methods: XPS with ion etching and FIB-SEM analysis.

## 2.1 Estimation based on XPS erosion rate

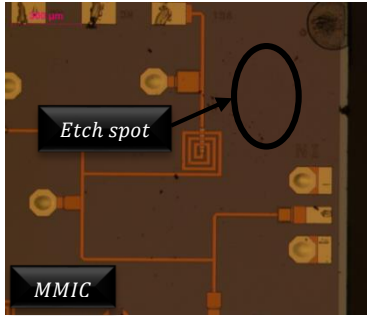


Figure 1: Etched spot position on GaAs MMIC for XPS and ion etching analysis.

XPS helps to make a quantitative analysis and extract the atomic ratio of each chemical element at the surface (hydrogen excepted). In the present case, it is combined with ion etching in order to measure the atomic ratio depth profile. The spot size of XPS beam is 200 $\mu\text{m}$ . Figure 1 shows the etched spot position on the die; a device-free area has been selected so that the layer sequence is GaAs/ $\text{SiN}_x$ / $\text{SiO}_y$ / $\text{SiN}_x$ .

The thicknesses of the superficial layers were obtained by splitting the XPS depth profile (Figure 2) in 3 areas:

external  $\text{SiN}_x$  (0-250s),  $\text{SiO}_y$  (250-1500s) and internal  $\text{SiN}_x$  (1500-1800s).

After 1800s of etch time, results show the rise of Ga and As peaks which means that GaAs substrate has been reached. This reveals that the experiment is successful.

With an etch rate around 0,6nm/s (pre-calibrated), the thicknesses of the different layers have been obtained easily with respectively 150nm for the external  $\text{SiN}_x$  (passivation layer), 750nm for the  $\text{SiO}_y$  dielectric and 180nm for the internal  $\text{SiN}_x$  in contact with GaAs.

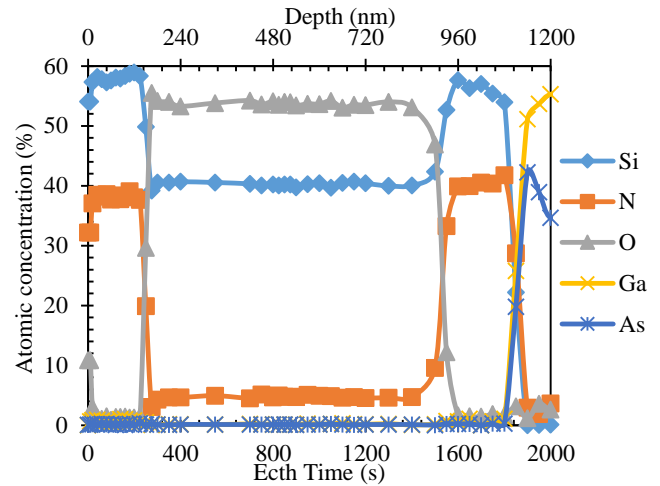
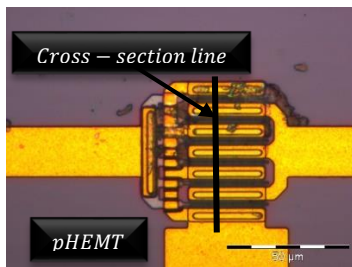
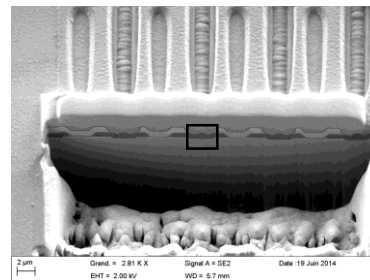


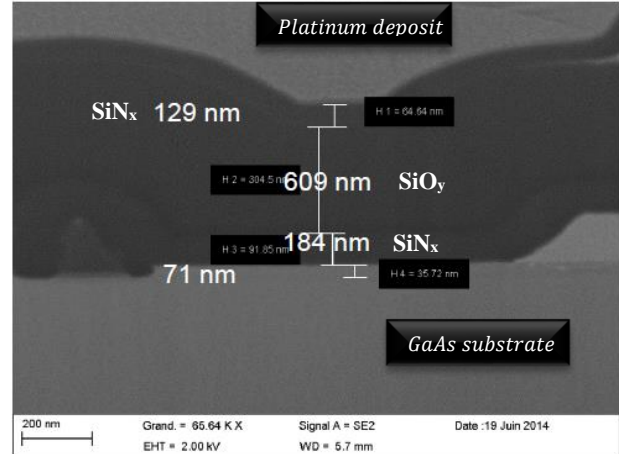
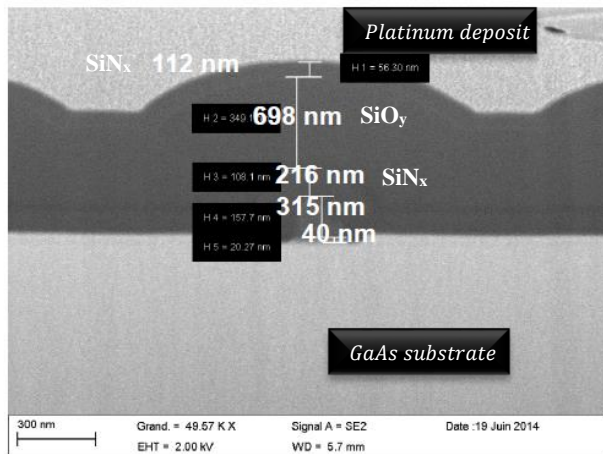
Figure 2: XPS depth profile for superficial layers on GaAs substrate



a. pHEMT surface observation by optical microscopy.



b. Gate fingers observation by SEM after FIB etching.



c. Cross-sections of pHEMT gate fingers with platinum deposit (FIB-SEM).

Figure 3: FIB-SEM analysis on GaAs MMIC.

The atomic ratio of silicon (Si) and nitrogen (N) in two SiN<sub>x</sub> layers is practically the same but it cannot be concluded definitely that the two layers are of the same quality; in particular the hydrogen content could be different, which is very important for stress in the layer and the protection it offers. Ratio N/Si  $\approx$  0.06 between 250-1500s (SiO<sub>y</sub> zone), which means either that N is inserted in the SiO<sub>y</sub> layer or that the etching front is quite rough. Measurements have been repeated at different positions and on other samples, giving the same results.

## 2.2 FIB-SEM measurement

In the non-planar gate area, FIB-SEM is a more adequate technique to measure both metallic and insulating materials. Figures 3a and 3b show the cutting plane chosen to measure gate finger metal thicknesses, and a tilted SEM view of the cut. A Platinum (Pt) layer has been deposited to protect the surface during FIB ion milling. The die tilt is 30° in order to observe the bottom of the section. The experimental results are shown in Figure 3c. For the insulating layers, thickness is  $\sim$ 129nm for SiN<sub>x</sub> (passivation layer),  $\sim$ 698nm for SiO<sub>y</sub> dielectric and  $\sim$ 216nm for the internal SiN<sub>x</sub> layer. These values are in reasonable agreement with those deduced from XPS, resp. 150nm, 750nm and 180nm. Note that the areas measured by these two techniques are different and do not show necessarily the same thickness exactly.

The small differences between the predicted thicknesses (foundry datasheet: 800nm for SiO<sub>y</sub>, 150nm for SiN<sub>x</sub>) and those measured by XPS and FIB-SEM is explained by the fact that the deposition is chemical (PECVD: Plasma-Enhanced Chemical Vapor Deposition), so that geometrical singularities have a notable impact on local thicknesses. In the rest of this study, the datasheet thicknesses are considered confirmed and are used in the simulations.

## 3. Summary of analytic models[4][5] [6]

Residual stresses were first analyzed by Stoney [4] who considered a bilayer strip consisting of a film and substrate. He derived a simple equation to relate the stress in the film to the curvature of the strip. In the simple case where the film thickness is considered infinitesimal compared to the substrate thickness ( $t_s \gg t_f$ ), Nix [5] has used continuum mechanics laws and Stoney's assumptions to evaluate the thermo-mechanical stress induced in the film far from the edge by die heating from room temperature  $T_0$  to temperature  $T$ :

$$\sigma_f(T) = \frac{E_f}{1-\nu_f} (\alpha_s - \alpha_f) (T - T_0) \quad (1)$$

Where  $\alpha_s$  and  $\alpha_f$  are respectively the CTE of the substrate and the film.  $E_f$ ,  $\nu_f$  are the Young's modulus and the Poisson's ratio of the film.

Recently, a more complete, yet simple analytical model for analyzing thermal stresses and deformation in multilayers has been developed by Hsueh [6]. The multilayer is subjected to a temperature change  $\Delta T$ ; the CTE of the substrate and the films are  $\alpha_s$ , and  $\alpha_i$ ,

$i = 1 \dots n$  respectively. At positions away from the edge of the multilayer, the stresses induced by the CTE mismatch are in-plane (i.e., parallel to the interface) and equi-biaxial for the plane geometry. Both the stress normal to the interface and the interfacial shear stress are zero. The coordinate system is defined such that the layer 1 ( $i = 1$ ) and substrate interface is located at  $y = 0$ , the interface between layers  $i$  and  $i + 1$  is located at  $y = h_i$ . Here  $t_s$  and  $t_i$  are respectively the thickness of the substrate and the films. The free surfaces of the multilayer are located at  $y = -t_s$  and  $y = h_n$ . The position in  $y$  axis is obtained with  $h_i = \sum_{j=1}^i t_j$ .

The in-plane biaxial stress distributions in the substrate and layers,  $\sigma_s$  and  $\sigma_i$  can be expressed as:

$$\sigma_s = \frac{E_s}{1-\nu_s} \left( c + \frac{y-b}{r} - \alpha_s \Delta T \right) \quad (\text{for } -t_s \leq y \leq 0) \quad (2a)$$

$$\sigma_i = \frac{E_i}{1-\nu_i} \left( c + \frac{y-b}{r} - \alpha_i \Delta T \right) \quad (\text{for } i = 1 \text{ to } n) \quad (2b)$$

The three parameters  $c$ ,  $b$ , and  $r$  are respectively the uniform strain component, the position of the bending axis at which the bending strain component is zero and the radius of curvature of the system. They can be obtained by applying the three boundary conditions: (i) the resultant force due to the uniform strain component is zero, (ii) the resultant force due to the bending strain component is zero, (iii) the resultant bending moment due to the stresses described by equation (2a) and (2b) is zero.

$$c = \frac{(E_s' t_s \alpha_s + \sum_{i=1}^n E_i' t_i \alpha_i) \Delta T}{E_s' t_s + \sum_{i=1}^n E_i' t_i} \quad (3a)$$

$$b = \frac{-E_s' t_s^2 + \sum_{i=1}^n E_i' t_i (2h_{i-1} + t_i)}{2(E_s' t_s + \sum_{i=1}^n E_i' t_i)} \quad (3b)$$

$$\frac{1}{r} = \frac{3[E_s'(c - \alpha_s \Delta T)t_s^2 - \sum_{i=1}^n E_i' t_i (c - \alpha_i \Delta T)(2h_{i-1} + t_i)]}{E_s' t_s^2 (2t_s + 3b) + \sum_{i=1}^n E_i' t_i [6h_{i-1}^2 + 6h_{i-1}t_i + 2t_i^2 - 3b(2h_{i-1} + t_i)]} \quad (3c)$$

Knowing the value of  $c$ ,  $b$  and  $r$ , the general solutions for the stress distributions  $\sigma_s$  and  $\sigma_i$  in the multilayer given by equations (2a) et (2b) are complete.

## 4. Numerical models

This section focuses on a description of the numerical models. Finite element simulations were performed using Abaqus Standard Software. Two geometrical models have been presented:

- “simple case” considering the whole die as a planar multilayer stack on substrate (Figure 5,6).
- the second “complete model” takes into account the gate area and geometrical singularity (Figure 7).

A structured mesh composed of linear elements has been built. Because of the in-plane stress simplification, simulation was carried out in 2D and due to geometrical symmetries, only half of the multilayer was modeled. The contacts are assumed to be tie elements.

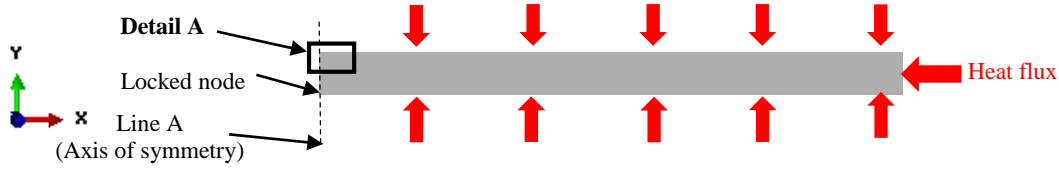


Figure 4: 2D modeling of half die with Abaqus CAE.

Regarding boundary conditions and symmetries, the node ( $x = 0$  and  $y = -t_s$ ) was locked and the normal displacement of Line A set at zero as shown in Figure 4.

In case gate current is present, a local heat source due to the current flow must be taken into account. However here, since THB tests use the reverse biasing on the transistor, the current flow in the gate is locked and there is no internal heat source. Therefore, the flux is considered homogeneous all around the die (Figure 4). The heating condition was a uniform thermal flux on the external surface, applied from room temperature ( $\sim 22^\circ\text{C}$ ) to test temperature ( $85^\circ\text{C}$ ). In the range  $22^\circ\text{C}$ - $85^\circ\text{C}$  variations of materials properties are considered negligible and simulations were performed under linear elastic theory. For the input data resumed in Table 1, the values came from bibliography [7] [8].

FEA materials description is more extensive than in previous analytical models: thermal conductivity, heat capacity and density have been added. The contact at the interface is supposed to be perfect. The following thicknesses are used in modeling: 150nm  $\text{SiN}_x$ , 800nm  $\text{SiO}_y$ , 20nm Ti, 140nm Al, 20nm Au and  $100\mu\text{m}$  GaAs substrate.

Table 1: Materials properties [7] [8]

Properties	Materials					
	AsGa	$\text{SiN}_x$	$\text{SiO}_y$	Ti	Al	Au
Young's modulus (GPa)	85.5	150	79.2	114	69	78
Poisson's ratio	0.31	0.3	0.22	0.34	0.34	0.42
CTE ( $10^{-6}/\text{K}$ )	6.86	3	0.55	8.4	23	14.2

#### 4.1 Simple case

In the simple case, two models have been used for simulations. First, the die is considered as a multilayer with a stack of  $\text{GaAs}/\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  because it represents a typical cross-section of the free surface of the GaAs microwave (see Figure 5).

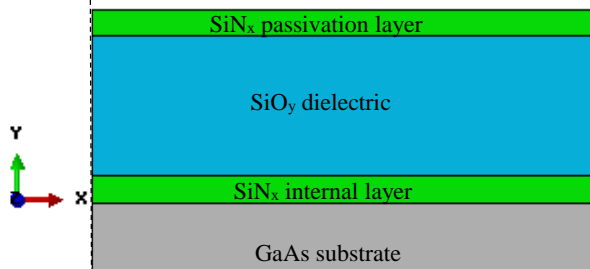


Figure 5: Detail A in the simple case.  
Stack  $\text{GaAs}/\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$

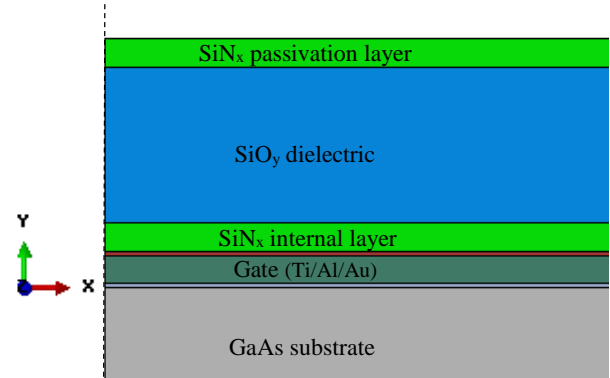


Figure 6: Detail A in the simple case.  
Stack  $\text{GaAs}/\text{Ti}/\text{Al}/\text{Au}/\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$

Second, calculations are made with a stack of  $\text{GaAs}/\text{Ti}/\text{Al}/\text{Au}/\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  representing the surface topography in gate finger areas without geometrical singularities.

#### 4.2 Complex case

In reality, geometrical singularities (transistor, capacitor, resistor, interconnections, air bridge...) in the active areas of the chip represent  $\sim 30\%$  of the surface topography.

For the complex model, one finger of the  $0,18\mu\text{m}$  pHEMT gate has been defined as a multilayer of  $\text{Ti}/\text{Al}/\text{Au}$  stack. Above this, there is a  $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  stack. Gate length and width details were drawn from the previous FIB-MEB cross-sections.

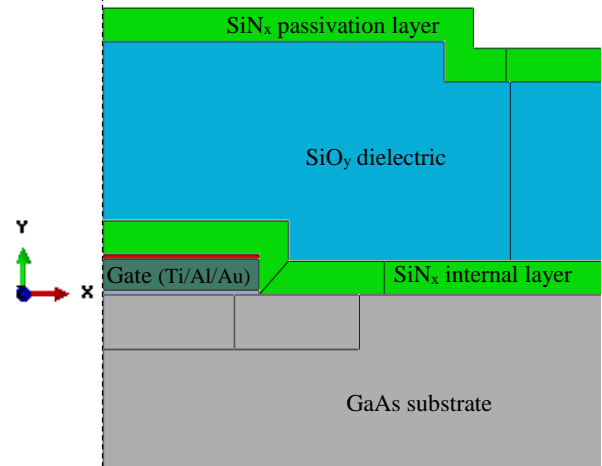


Figure 7: Detail A in the complex case.  
Typical cross-section of GaAs pHEMT gate in contact areas.

## 5. Results

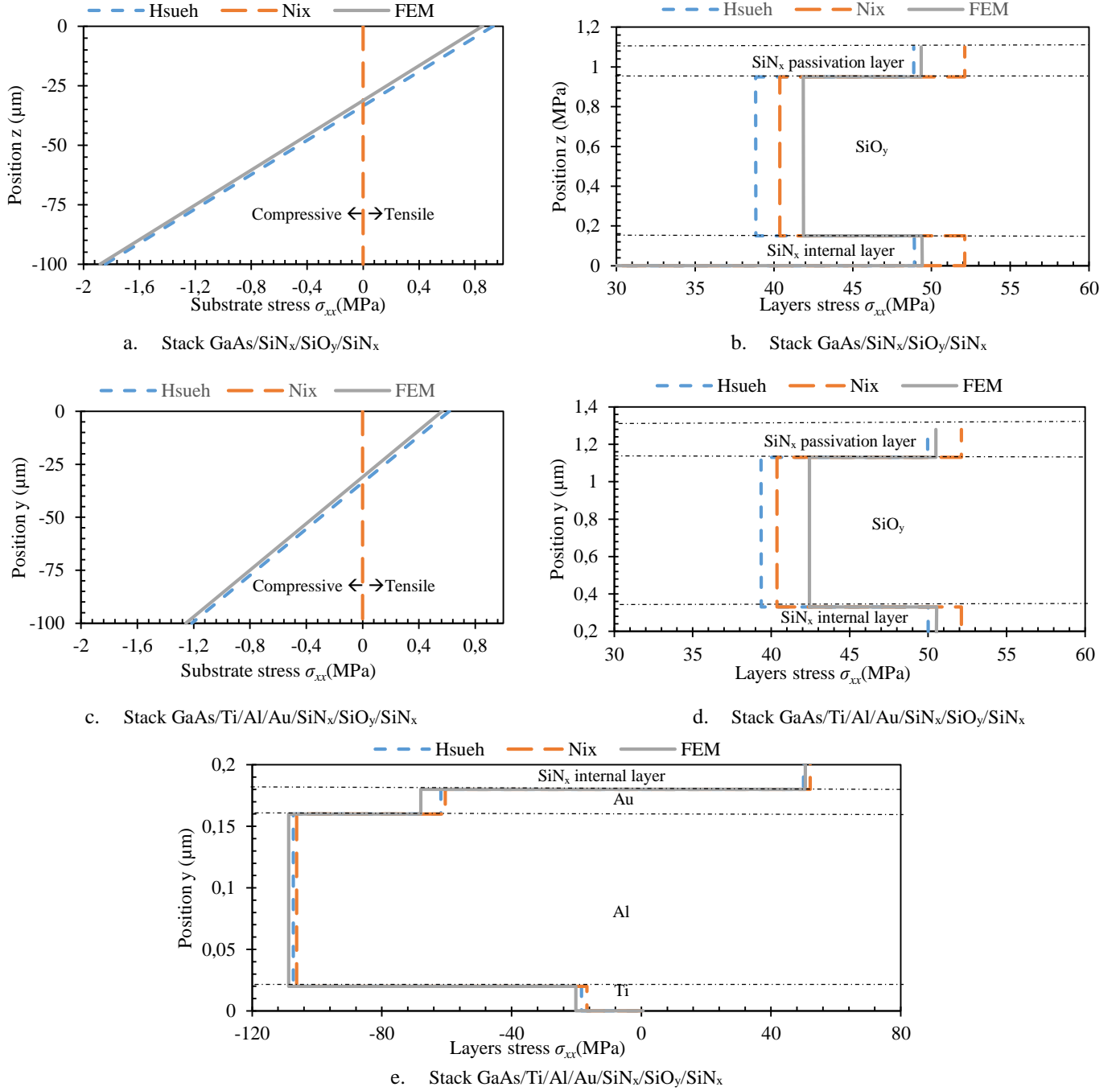


Figure 8: Comparison between Hsueh, Nix and Abaqus FEM results: Biaxial thermo-mechanical stress  $\sigma_{xx}$  distribution through the thickness of (a), (c) the substrate and (b), (d), (e) the thin film layers.  $x=0$  at the interface GaAs/SiN<sub>x</sub> and GaAs/Ti

Thermo-mechanical stresses induced by THB 85/85 aging tests have been evaluated in a reverse biasing case (no gate finger warming).

The induced stresses (with  $\Delta T = 63^\circ\text{C}$ ) for Nix and Hsueh models through the thickness of the system (Figure 5,6) are calculated from equations (1), (2a) and (2b). In order to examine the accuracy of these results, Abaqus FEA simulations have been performed

(Figure 5, 6 and 7) with the same dimensional and materials properties. In the calculation, Abaqus FEA has been used for the two simple configurations represented on Figures 5, 6 and compared to Nix and Hsueh methods which are usually used in the literature. Then for the “complex” case shown in Figure 7, only Abaqus FEA has been done in order to complete our analysis.



The  $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  stack directly deposited on the GaAs substrate as shown in Figure 5 represents the configuration about ~70% of the die surface (Figure 1). Each layer has its specificity: the bottom  $\text{SiN}_x$  acts as insulator, the  $\text{SiO}_y$  is the dielectric for MIM capacitors and the upper  $\text{SiN}_x$  layer is the die passivation layer. By considering this cross-section, the thermo-mechanical stresses through the thickness of this stack for Hsueh, Nix and Abaqus FEA models are shown in Figure 8b. The three layers are in tensile stresses ( $\sigma_{xx}$  component) because for each layer the CTE is lower than for the GaAs. For the same layer, the stress induced at the lower surface is always less tensile than the stress at the upper surface. The results obtained indicate tensile stresses in the internal  $\text{SiN}_x$ , the  $\text{SiO}_y$  dielectric and the  $\text{SiN}_x$  passivation layer respectively 50MPa, 42MPa and 50MPa. In the substrate, induced stress distribution is shown in Figure 8a. According to Hsueh and Abaqus FEA results, the top surface ( $y = 0$ ) is subjected to tension and the bottom ( $y = -t_s$ ) is subjected to compression. As it has been considered in the assumptions for Nix's model ( $t_s \gg t_i$  and  $\sigma_s \approx 0$ ), the stress induced in the substrate is supposed negligible.

A second stack of GaAs/Ti/Al/Au/ $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  shown in Figure 6 is used to evaluate the induced stress in the gate metallization of the transistors. In this stack, the inserted Ti/Al/Au layers representing the gate fingers are subjected to compression because they have a higher CTE than GaAs. Mainly among these three layers, Aluminum (Al) is subjected to high compression because its CTE is higher than Ti and Au. Comparisons of thermo-mechanical stresses in the gate fingers evaluated by different methods are shown in Figure 8e. It should be noted that the thermo-mechanical stresses in the gate metal (Al), Ti and Au are compressive and respectively around -108MPa, -30MPa and -68MPa. According to Figure 8c, the induced stress in the substrate for this stack is in tension at the top surface and in compression at the bottom.

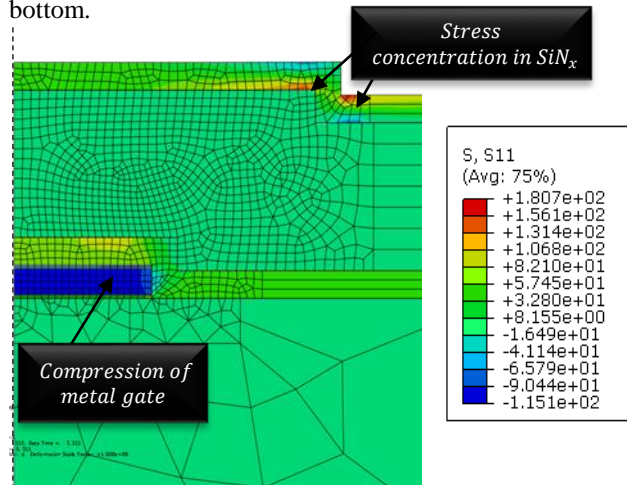


Figure 9: Thermo-mechanical stresses  $\sigma_{xx}$  simulated with Abaqus in the gate finger area (Detail A) for complex case.

For the complex case (Figure 7), simulation results with Abaqus FEA model shown in Figure 9 indicate a tensile stress concentration up to 181MPa in the  $\text{SiN}_x$  passivation layer, and a stress level of 110MPa for the internal  $\text{SiN}_x$  layer. The induced stress in the substrate for this configuration is the same as shown in Figure 8c.

## 6. Discussion

Results from the previous section show the thermo-mechanical stress induced in the GaAs microwave devices by the temperature raise during THB 85°C/85RH testing. Each one of the three methods used has its particularities. Nix's formulation is helpful as a first approximation because of its simplicity (equation 1); Hsueh's equations are a more precise by including the thicknesses and all the details on the films deposited, finally the Abaqus FEA is the only one that can take into account geometrical singularities and include more materials properties.

For the flat layers, the differences are quite small, a few MPa at most except in the substrate where the averaged Nix's stress does not show the gradient. Let us compare for instance Hsueh and Abaqus FEA results for the stack GaAs/Ti/Al/Au/ $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  (Figure 8c,d) with the outcomes from stack GaAs/ $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$  (Figure 8a,b). With the additional metallic layers (Ti/Al/Au), stress in the GaAs substrate decreases by about 40% compared with ( $\text{SiN}_x/\text{SiO}_y/\text{SiN}_x$ ). This is explained by the negative sign of  $\Delta\alpha = (\alpha_s - \alpha_f)$  for each inserted thin film. However stress in the thick substrate is very small in all cases (<2MPa).

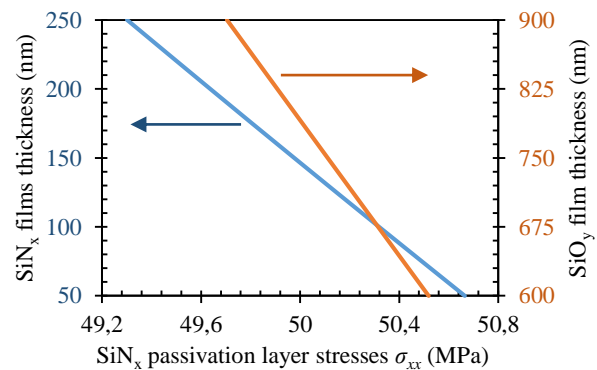


Figure 10: Thermo-mechanical stresses  $\sigma_{xx}$  evaluated with Hsueh's method in the  $\text{SiN}_x$  passivation for different thicknesses of  $\text{SiN}_x$  and  $\text{SiO}_y$

A variability of thickness of the thin films ( $\text{SiN}_x$  and  $\text{SiO}_y$ ) has been observed in the FIB-SEM cross-sections (Figure 3c). An investigation of its effect on the induced stresses has been made using the model presented in Figure 6. According to Hsueh's model results shown in Figure 10, the stress in the  $\text{SiN}_x$  external passivation layer hardly changes (<3%) when the thicknesses of the other two are decreased even strongly. This low variation is explained by the condition:  $t_s \gg t_i$  so that the substrate behavior dominates.

A comparison of the thermo-mechanical stresses simulated with Abaqus FEA in a simple (Figure 8b) and complex (Figure 9) cases shows similar results in the metallic gate (-108MPa in simple case and -115MPa in the complex case). However the tensile stress in the SiN<sub>x</sub> passivation layer is strongly affected by geometrical singularities which induce stress concentration areas: from +50 MPa in the simple case, it jump to more than 150MPa near the step, which might have consequences on the integrity of the layer.

Failure analysis of GaAs device under THB 85/85 aging testing has revealed that damages were caused mainly by the degradation of passivation layer (cracks, diffusion...) [9] [10] which leads to moisture intrusion in the die followed by corrosion. In a previous work on the same technology of GaAs microwave [2], several cracks have been observed in the SiN<sub>x</sub> passivation layer (Figure 11) and also in the gate metal (Figure 12). This crack induces a large degradation of drain current monitored during THB test.

Indeed, the temperature change and aggressive environment induce stresses which must be added to the existing residual stresses from fabrication. In our specific case (Figure 7), by evaluating the thermo-mechanical stresses induced by heating from room temperature to 85°C, it should be noticed that the stress concentration

areas (Figure 9) are very similar to cracked areas (Figure 11). This result suggests leads us to claim that the failure of the passivation layer is directed linked to architectural failure and thermo-mechanical stresses must be considered in the failure analysis. The author [2] also explains these failures (Figure 12) by the existing internal stresses added to the induced stresses (thermo-mechanical and hydro-mechanical stresses).

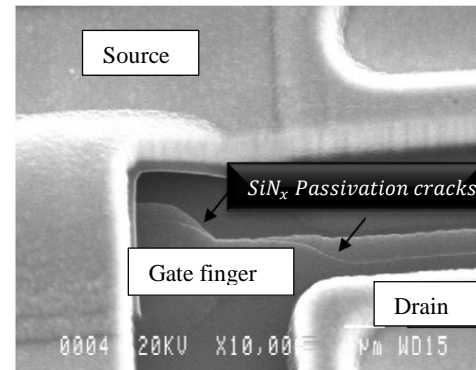


Figure 11: Damages of GaAs die after 3000 hours at 85°C/85%RH without bias [2]: SEM observation of gate finger, drain and source contacts

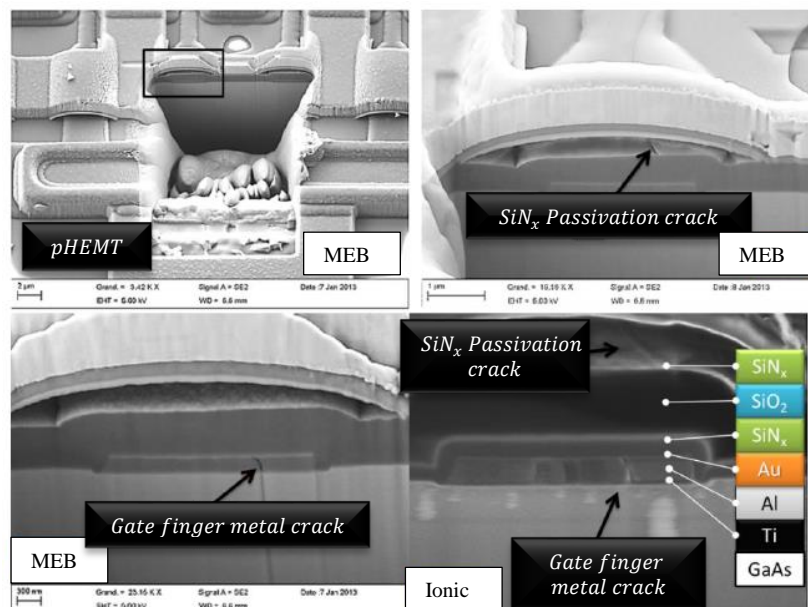


Figure 12 : Damages of GaAs die after 672 hours at 85°C/85%RH in reverse bias [2] : Cross-section of pHEMT gate finger

Due to the linearity of stress state, any initial stress state, once determined, can simply be added to the results presented.

## 7. Conclusions

Coefficients of thermal expansion mismatch between layers induces internal stress in multilayers thin films on substrate. These residual stresses in multilayer systems influence their reliability and can result in cracking.

In the present analysis, the thermo-mechanical stress induced in thin films of GaAs microwave under THB testing is evaluated by heating from room temperature to test temperature. Analytical models [5] [6] have been used to make analysis and the FEA has been used for results validation.

With a model that takes into account the geometrical singularities and the thickness of layers (Figure 7) in the



pHEMT gate fingers (Ti/Al/Au), FE simulations indicate compression of metal gate (Al) reaching -115MPa. This is due to its higher CTE with respect to the surrounding SiN<sub>x</sub>. Inversely, the SiN<sub>x</sub> passivation experiences up to 181MPa when its geometric singularities are taken into account. These results have been correlated with the cracks areas observed previously [2] on non-hermetic tested devices under reverse bias. This proves the usefulness of thermo-mechanical analysis to complete failure analysis under THB aging life test. It should be considered in further analysis of the reliability of active microwave devices.

In view of accurate evaluation, further investigation should determine the main properties of die thin films (SiN<sub>x</sub>, SiO<sub>y</sub>...) by using ultrasonic measurements method on dice.

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